TI-24317

TOSHIBA 0862860

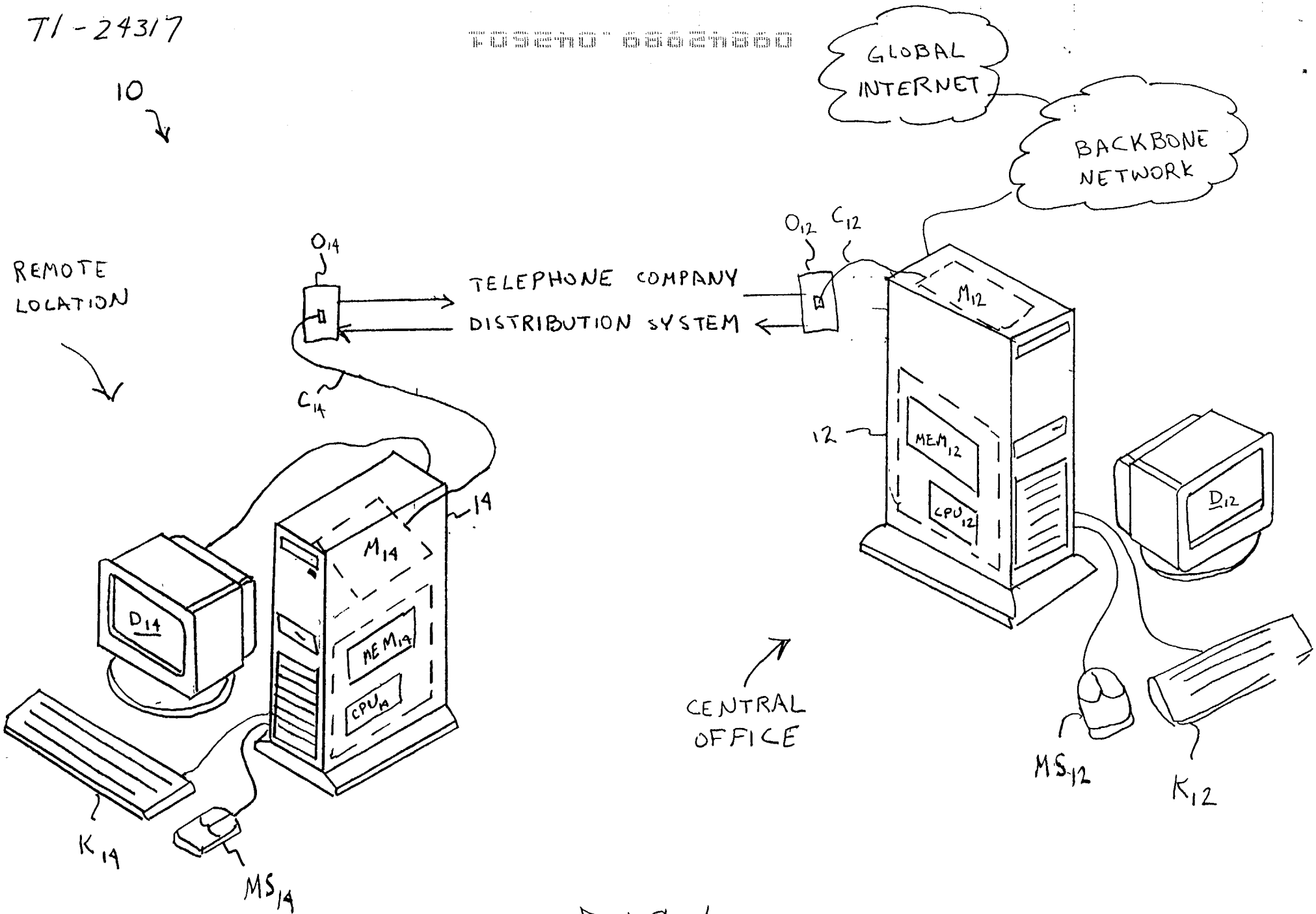
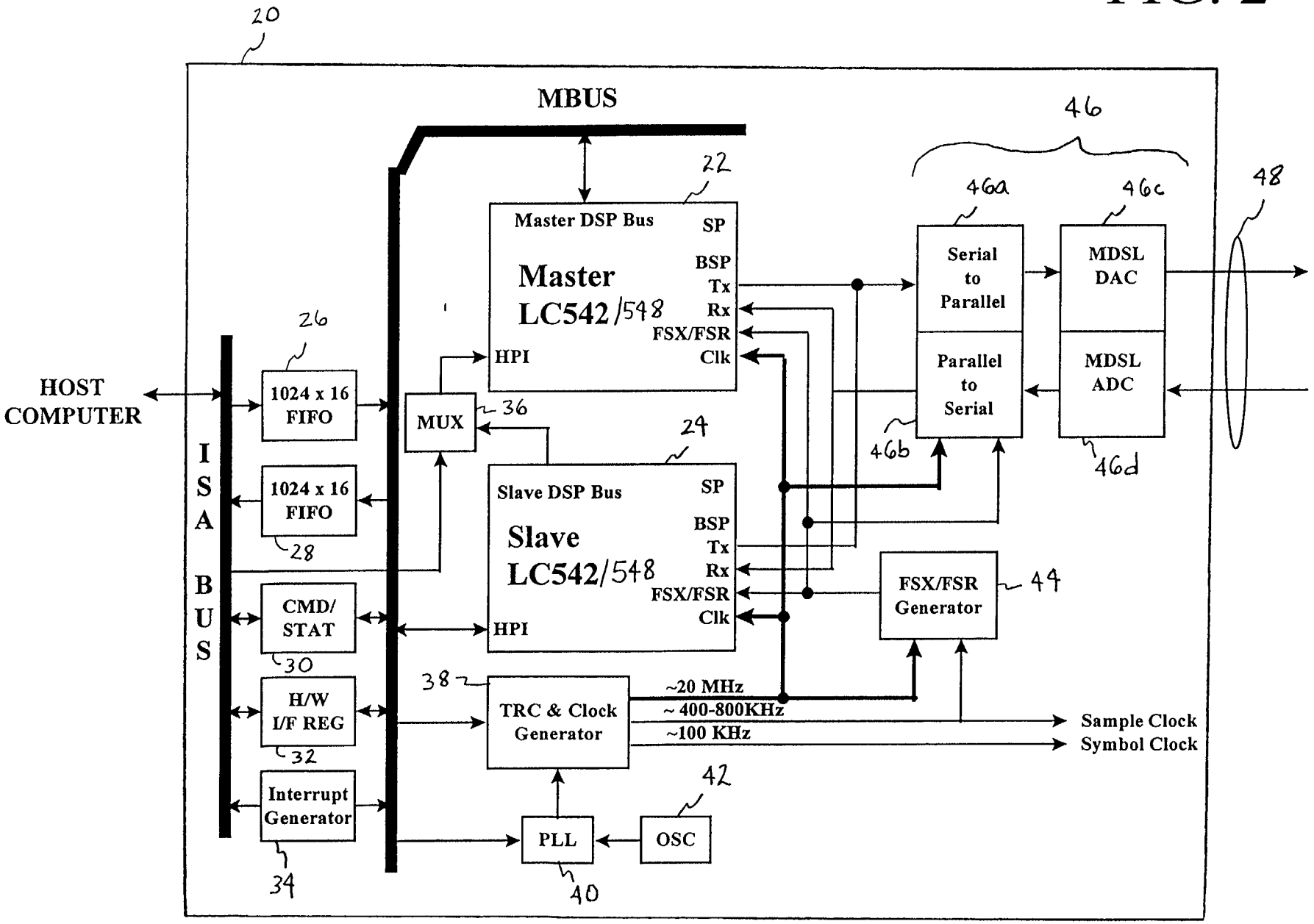


FIG. 1

FIG. 2


20
MBUS
46
22
46a
46c
48
Master DSP Bus
SP
Master
LC542/548
BSP
Tx
Rx
FSX/FSR
Clk
HPI
Serial
to
Parallel
MDSL
DAC
Parallel
to
Serial
MDSL
ADC
26
HOST
COMPUTER
1024 x 16
FIFO
MUX
36
24
46b
46d
ISA
BUS
1024 x 16
FIFO
28
Slave DSP Bus
SP
Slave
LC542/548
BSP
Tx
Rx
FSX/FSR
Clk
HPI
FSX/FSR
Generator
44
CMD/
STAT
30
38
H/W
I/F REG
32
TRC & Clock
Generator
~20 MHz
~ 400-800KHz
~100 KHz
Sample Clock
Symbol Clock
Interrupt
Generator
34
42
PLL
OSC
40

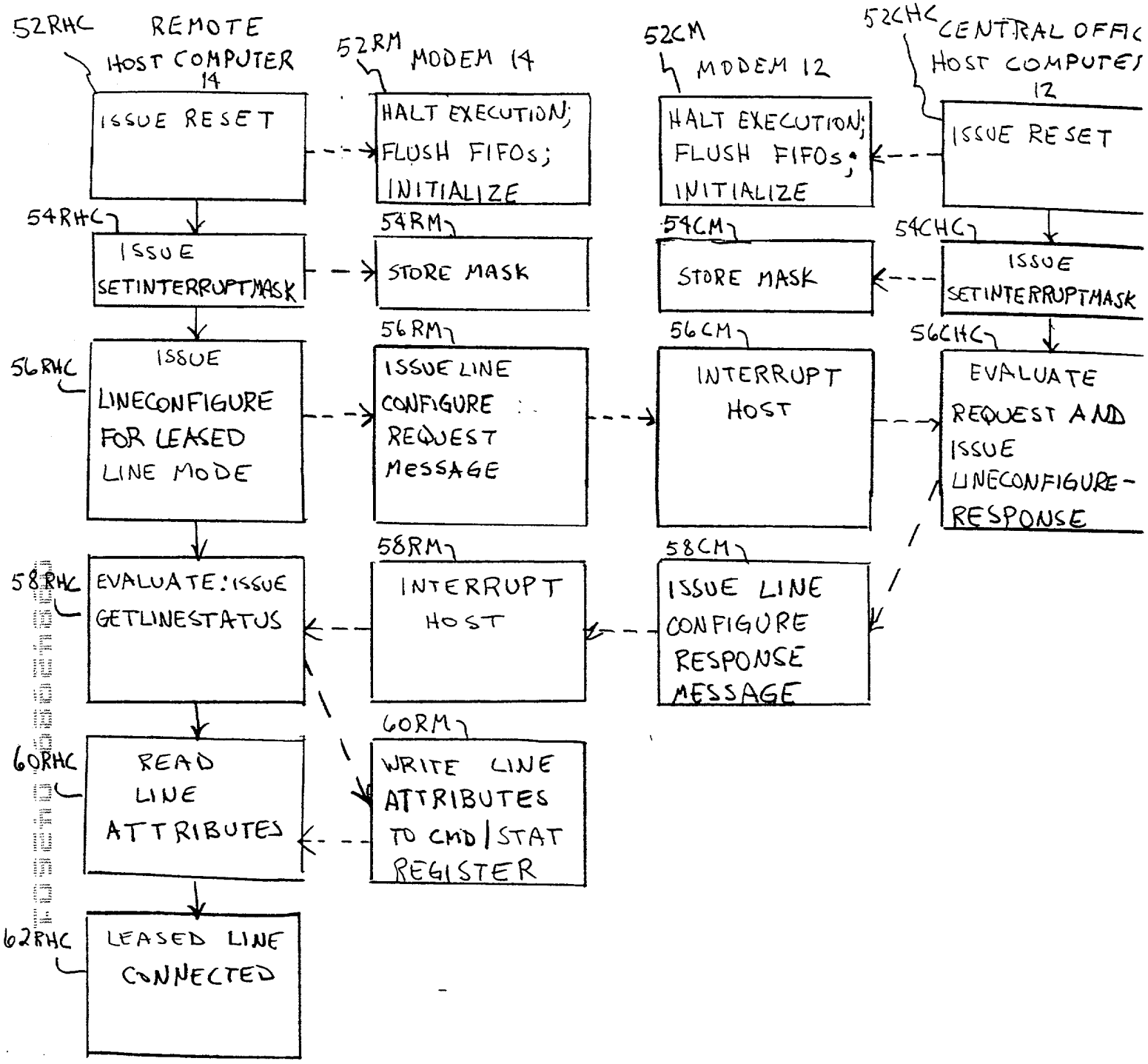

52RHC
REMOTE HOST COMPUTER 14
52RM
MODEM 14
52CM
MODEM 12
52CHC
CENTRAL OFFIC HOST COMPUTE 12
ISSUE RESET
HALT EXECUTION; FLUSH FIFOs; INITIALIZE
HALT EXECUTION; FLUSH FIFOs; INITIALIZE
ISSUE RESET
54RHC
ISSUE SETINTERRUPTMASK
54RM
STORE MASK
54CM
STORE MASK
54CHC
ISSUE SETINTERRUPTMASK
56RHC
ISSUE LINECONFIGURE FOR LEASED LINE MODE
56RM
ISSUE LINE CONFIGURE REQUEST MESSAGE
56CM
INTERRUPT HOST
56CHC
EVALUATE REQUEST AND ISSUE LINECONFIGURE-RESPONSE
58RHC
EVALUATE: ISSUE GETLINESTATUS
58RM
INTERRUPT HOST
58CM
ISSUE LINE CONFIGURE RESPONSE MESSAGE
60RM
WRITE LINE ATTRIBUTES TO CMD/STAT REGISTER
60RHC
READ LINE ATTRIBUTES
62RHC
LEASED LINE CONNECTED

FIG. 3

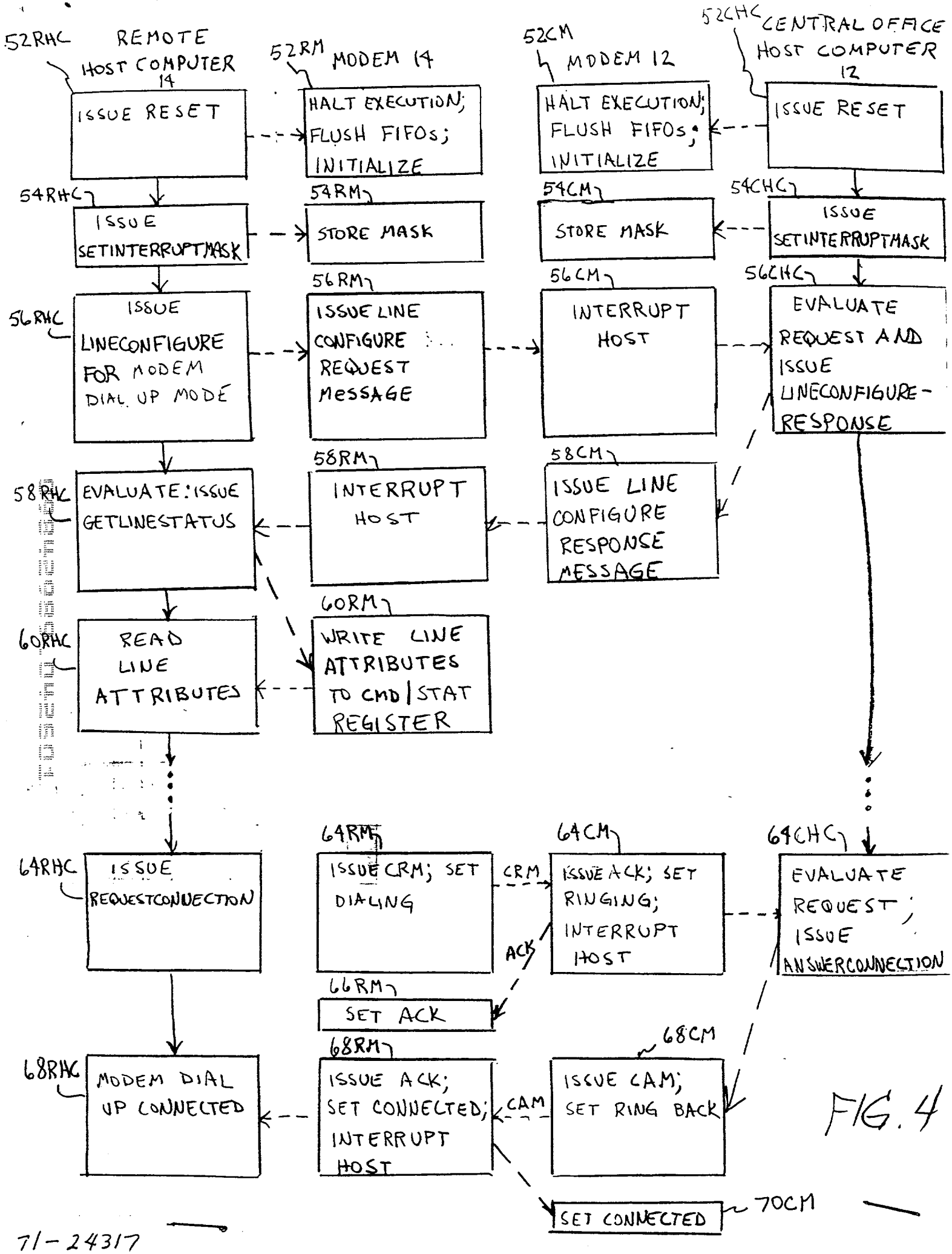


FIG. 4

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